Oscillator Terms and Application Notes

TECHNICAL TERMS

Nominal frequency: The center or nominal output frequency of a crystal oscillator.

Package: Crystal oscillators are packaged in various styles from lead through holes to surface-mount types. Various sizes and functions are suitable for different applications.

Frequency tolerance: The deviation from the nominal frequency in terms of parts per millions (ppm) at room temperature. (25° ± 5°C)

Frequency range: The frequency band that the oscillator type or model can be offered.

Frequency stability: The maximum allowable frequency deviation compared to the measured frequency at 25°C over the temperature window, i.e., 0°C to +70° C. The typical stability is ± 0.01% (±100 ppm).

Operating temperature: Temperature range within which output frequency and other electrical, environmental characteristics meet the specifications.

Aging: The relative frequency change over a certain period of time. This rate of change of frequency is normally exponential in character. Typically, aging is ± 5ppm over 1 year maximum.

Storage temperature: The temperature range within which the unit is safely stored without damaging or changing the performance of the unit.

Frequency vs. power supply variation: Maximum frequency change allowed when the power supply voltage is changed within its specified limits (typical ±10% in Vcc or ±5% change).

Supply voltage (Vdd max): The maximum voltage which can safely be applied to the Vcc terminal with respect to ground. Maximum supply voltage for TTL is 5.5V and for HCMOS is 6V.

Input voltage (V_{IN}): The maximum voltage that can be safely applied to any input terminal of the oscillator.

Output HIGH voltage(V_{OH}): The minimum voltage at an output of the oscillator under proper loading.

Output LOW voltage (V_{OL}): The maximum voltage at an output of the oscillator under proper loading.

Input HIGH voltage (V_{IH}): The minimum voltage to guarantee threshold trigger at the input of the oscillator.

Input LOW voltage(V_{IL}): The maximum voltage to guarantee the threshold trigger at the input of the oscillator.

Supply current (Icc): The current flowing into Vcc terminal with respect to ground. Typical supply current is measured without load.

Symmetry or duty cycle: The symmetry of the output wave form at the specified level (at 1.4V for TTL, at 1/2Vcc for HCMOS, or 1/2 waveform peak level for ECL).
SYM =TH/T x 100 (%); See Fig. 1.

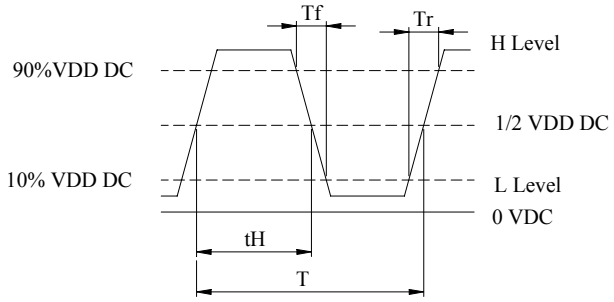

Figure 1

Rise time (T_r): Waveform rise time from Low to High transition, measured at the specified level (20% to 80% for HCMOS, ECL, and 0.4V to 2.4V for TTL).

Fall time (T_f): The waveform fall time from High to Low transition, measured at the specified level (80% to 20% for HCMOS, ECL, and 2.4V to 0.4V for TTL).

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Fan out: The measure of driving ability of an oscillator, expressed as the number of inputs that can be driven by a single output. It can be represented by an equivalent load capacitance (C_L) or a TTL load circuit consisting of diodes, load resistor, and a capacitor.

Jitter: The modulation in phase or frequency of the oscillator output.

HCMOS/TTL compatible: The oscillator is designed with ACMOS logic with driving capability of TTL and HCMOS loads while maintaining minimum logic HIGH of the HCMOS.

Tristate enable: When the input is left OPEN or tied to logic "l", the normal oscillation occurs. When the input is Grounded (tied to logic "0"), the output is in HIGH IMPEDANCE state. The input has an internal pull-up resistor thus allowing the input to be left open.

Output logic: The output of an oscillator is designed to meet various specified logics, such as TTL, HCMOS, ECL, Sine, Clipped-Sine (DC cut).

Harmonic distortion: The non-linear distortion due to unwanted harmonic spectrum component related with target signal frequency. Each harmonic component is the ratio of electric power against desired signal output electric power and is expressed in terms of dBc, i.e. -20dBc. Harmonic distortion specification is important especially in sine output when a clean and less distorted signal is required.

Phase noise: The measure of the short-term frequency fluctuations of the oscillator. It is usually specified as the single side band (SSB) power density in a 1 Hz bandwidth at a specified offset frequency from the carrier. It is measured in dBc/Hz.

Standby: A function that temporary turns off the oscillator and other dividers to save power. Logic "0" will enable stand by mode. The disable current at stand by mode varies from few microamperes to tens of microamperes (5pA typical). Because oscillation is halted, there is a maximum of 10 ms (same amount of start-up time) before output stabilizes.

OSCILLATORS APPLICATION NOTES

An oscillator is a circuit which produces a continuous output signal; thus it is called a signal generator. When the signal produced is a sine wave of constant amplitude and frequency, the oscillator circuit is called a sine wave generator. The oscillator can produce a square wave signal in digital logic families such as TTL, CMOS, or ECL.

An oscillator can be divided into three definite sections:

(1) an amplifier
(2) the feedback connections
(3) the frequency determining components.

REQUIREMENTS FOR OSCILLATION

A circuit will oscillate if it consists of two minimum requirements:

(1)Positive feedback
(2)Loop gain greater than 1

Feedback is provided when we connect the output of an amplifier to its input. If the output fed back is 'out of phase' with the input, then the circuit has *negative feedback* (NFB). if the feedback from the output is in phase with the input, the circuit has *positive feedback* (PFB).

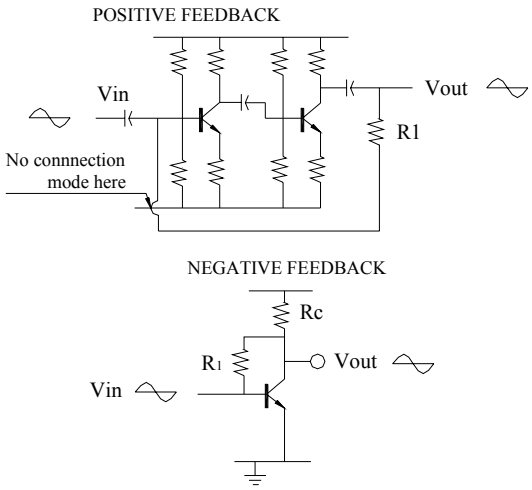

Figure 2

WELL KNOWN PIERCE OSCILLATOR CIRCUIT

Advantages:

(1) Operate at or near series resonance (about 5ppm to 40ppm from Fs).
(2) Very good short-term stability.

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(3) Work at any frequency from 1 kHz to 200MHz.
(4) Circuit provides a large output signal.
(5) Drives the crystal at a low power level.
(6) Oscillation frequency almost insensitive to small changes in the series resistance or shunt capacitance.

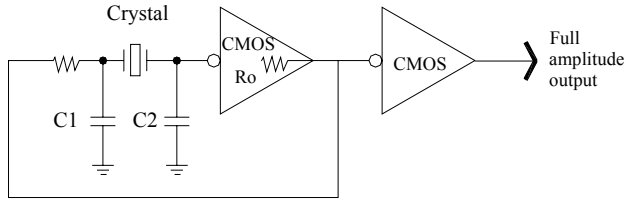

Figure 3. Pierce Oscillator Circuit

Circuit configuration:
•In most Pierce circuits, the amplifier consists of just one transistor. The output can be buffered out to a digital logic gate TTL, or CMOS.

•The Pierce amplifier can be designed with digital logic elements in CMOS, TTL, and ECL; CMOS for low frequencies, TTL for medium frequencies, and ECL for high frequencies.

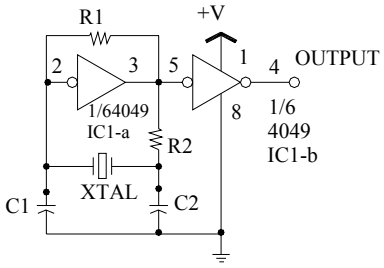

Figure 4

TRISTATE CONTROL IN CRYSTAL OSSCILLATORS

DIGITAL STATE LEVELS

Most digital systems use the binary number system represented by two state levels 0 and 1. In some special applications, a third-state (Hi Impedance output) is required.

APPLICATIONS

A three-state output, or tristate enable/disable function is available in TTL, HCMOS, or TRUHCMOS crystal oscillators. Its common applications include automated testing, bus wiring data transfer.

HOW TRISTATE WORKS?

The three states are low, high, and high impedance (Hi Z or floating). An output in the hi-impedance state behaves as if it is disconnected from the circuit except for possibly a small leakage current. Three-state devices have an enable/disable input, usually on pin 1 of almost any package. When enable is high or left floating, the device oscillates (with high and low outputs), and when pin 1 is grounded (logic "0"), the device goes into its high-impedance state.

A bus is a common set of wires, usually used for data transfer. A three-state bus has several three-state outputs wired together. With control circuitry, all devices on the bus except one have outputs in the high impedance state. The remaining device is enabled, driving the bus with high and low outputs.

Other applications for a tristate function are for Automated Testing Equipment (ATE). Outputs of several oscillators are wired together.

With control circuitry, all oscillators but one have outputs in the high impedance state. The only oscillator which is selected will have its frequency read out from the counter. (Fig. 5)

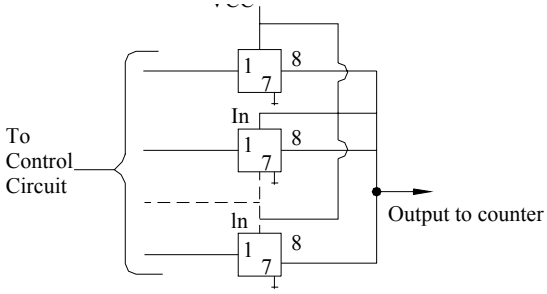

Figure 5

There is always some delay before the tristate function goes into effect. This effect occurs on both transitions (at disable and at

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enable). The output disable time of a tristate from LOW level is t_{PLZ} and the output enable time of a tristate to LOW level is t_{PZL}. (Fig. 6)

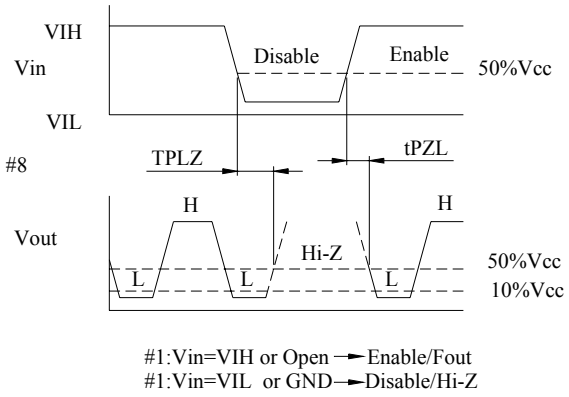

Figure 6

CMOS RISE AND FALL TIMES

The rise and fall time on the CMOS technology depends on its speed (CMOS, HCMOS, ACMOS, and BICMOS), the supply voltage, the load capacitance, and the load configuration. Typical rise and fall time for CMOS 40000 series is 30ns, HCMOS is 6ns, and for ACMOS (HCMOS, TTL compatible) is 3 ns max.
Typical rise and fall time is measured between 10% to 90% of its waveform level. (See Fig. 7)

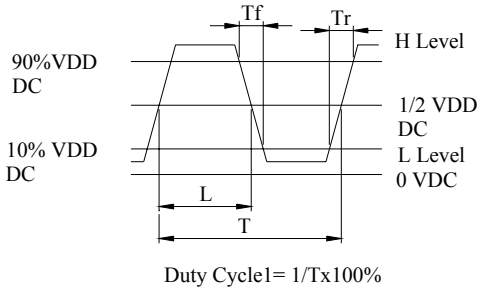

Figure 7

ACMOS OUTPUT TERMINATION TECHNIQUES

Due to the fast transition time of the ACMOS (HCMOS/TTL compatible) device, proper termination techniques must be used when testing or measuring electrical performance characteristics.

Termination is usually used to solve the problem of voltage reflection, which essentially causes steps in clock waveforms, as well as overshoot and undershoot. Such effect could result in false clocking of data, as well as higher EMI and system noise.

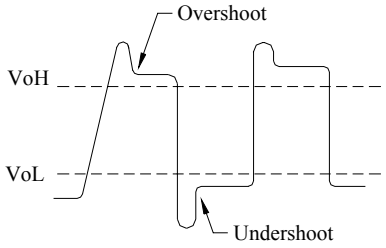

Figure 8

Termination is required also because of the length of the trace on the PC board and its load configuration.

There are three general methods of terminating a clock trace, which is a process of matching the output impedance of the device with the line impedance:

- Series termination
- Pull-up/Pull-down termination
- Parallel-AC termination

Method 1: Series termination (Fig. 9)

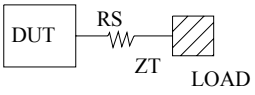

Figure 9

In series termination, a damping resistor is placed close to the source of the clock signal. Value of Rs must satisfy the following requirement:

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$$Rs \geq Z_T - Ro$$

Method 2: Pull-up/Pull-down resistors (Fig. 10)

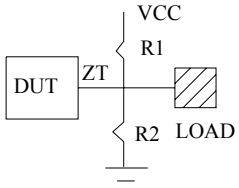

Figure 10

In pull-up/pull-down termination, the Thevenin's equivalent of the combination is equal to the characteristics impedance of the trace. This is probably the cleanest, and results in no reflections, as well as EMI.

$$RT \sim ZT$$

Method 3: Parallel AC termination (Fig. 11)

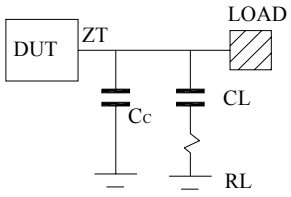

Figure 11

In parallel AC termination, an R-C combination is placed at the load. The value of the capacitor must be chosen carefully, usually smaller than the 5OpF. This termination is not recommended because it will degrade the rise and fall time of the clock, although it draws no DC current.

VCXO TECHNICAL TERMS

Control Voltage (Vc): An external voltage applied to the input of the VCXO. By changing the voltage, the frequency varies accordingly.
Typical Vc is 0V to 5V, 0.5V to 4.5V, -0.5V to -4.5 V

Deviation or frequency pullability: The minimum change in the output frequency with respect to the change in control voltage. Unit is measured in ppm. Standard pullability is ±50 ppm minimum, ±100 ppm minimum.

Maximum pullability: The maximum frequency change allowed for a maximum control voltage (for positive transfer function). Measured in ppm.

Transfer function: Direction of change in frequency vs. change in control voltage. The transfer is said to be positive if the frequency rises when increasing control voltage. The transfer function is negative if the frequency drops when increasing Vc.

Input Impedance: A measure of isolation between the input port of the VCXO network and the voltage control source. Typical Input impedance is >50kohms @ 10KHz.

Linearity: The deviation from the best straight line slope of the frequency vs. control voltage curve. Typical linearity is ±20% or ±10%.

Modulation bandwidth: The minimum ± 3dB bandwidth frequency, relative to a lKHz input modulation frequency.

Center frequency or nominal frequency: User specified frequency at center control voltage. Unit in Hz, kHz, MHz. Standard control voltage for center frequency is 2.5 V for a Vcc=5V.

VOLTAGE CONTROLLED CRYSTAL OSCILLATOR (VCXO)

VCXO is a voltage-controlled crystal oscillator. A VCXO has a voltage-variable (varactor) attached in series with the crystal. By varying the control voltage, the capacitance of the varactor changes accordingly, thus forces the frequency changed.

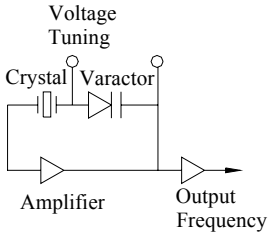

Figure12

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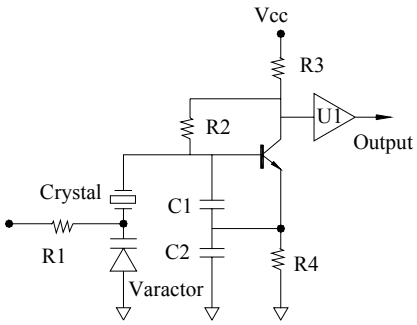

Figure 13

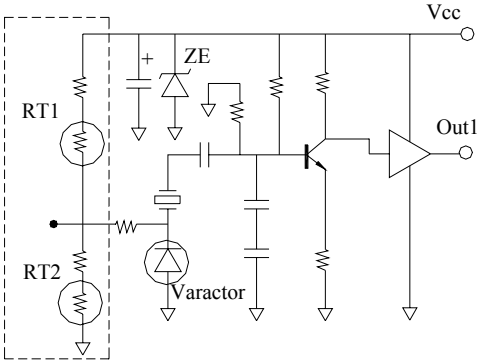

Figure 14

TEMPERATURE COMPENSATED CRYSTAL OSCILLATORS (TCXOS)

A temperature-compensated crystal oscillator is a crystal oscillator with a temperature-compensated network. The network consists of at least two (2) thermistors (temperature-variable resistors). The thermistors, which are very well selected during testing for temperature coefficient and values, are used to steer the control voltage in order to compensate the change in frequency over temperature. Temperature compensation can be achieved with or without use of a varactor. However, without varactor technique is harder to accomplish because exact resistors values have to be used to compensate.

Figure 8 shows a typical TCXO circuit with a thermistor network.

TCXO APPLICATIONS

Frequency Stability: Can achieve ±0.5 ppm to ±3 ppm.
Wide temperature available.
Used widely in various communications equipment (car phones, cordless phones, etc.), reference clocks, phase-locked loops (PLLs), signal tracking, cellular radios, aerospace, and other instrumentation.

External trimmer (mechanical) allows one to compensate frequency shift due to aging (±l ppm max. per year).

Voltage-controlled (analog) or digital TCXO (digital pulses) to correct frequency shift.

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